

NOTES (UNLESS OTHERWISE SPECIFIED):

1. BOARD FABRICATION METHODS MUST COMPLY WITH:  
FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X  
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS  
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. MATERIAL:  
NUMBER OF LAYERS: 2 LAYERS  
METAL 1 (TOP): 0.5oz. (1oz FINISHED)  
CORE 1: ROGERS 4003, (0.008in.) THICK  
METAL 2 (BOTTOM): 0.5oz. (1oz FINISHED)  
SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN.  
OR LDI (LASER DIRECT IMAGEABLE), GREEN.  
MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.  
SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:  
METAL 1 (TOP) AND METAL 2 (BOTTOM):  
ENEPIG PER IPC-4556  
NICKEL PLATE 118 - 236µin. (3 - 6µm).  
ELECTROLESS PALLADIUM 2 - 6µm. (0.05 - 0.15µm)  
IMMERSION GOLD (1.2 µin)
5. FINISHED BOARD THICKNESS: (0.011in.) ±0.003in.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM).
7. TOLERANCE: PC BOARD OUTLINE: ±0.003in.
8. BURRS SHALL NOT EXCEED 0.002in.
- 9 VIA PLATING/FILLING:  
A. VIAS 0.008in WITH SYMBOL "A" TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER  
THICKNESS TO BE 0.0007 ±0.00035in.  
B. ALL OTHER VIAS TO BE EPOXY-FILLED, SAN-EI KAGAKU PHP-900 NON-CONDUCTIVE EPOXY, PLANARIZED.  
C. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007 ±0.00035in. MIN. THICKNESS.
10. METAL1 (TOP) AND METAL2 (BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX  
ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.003in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST  
ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS: SINGLES
16. NO ELECTRICAL TEST NEEDED.

LAYER STACK LEGEND



DRILL TABLE

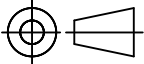
Symbol	Count	Hole Size	Plated	Via / Pad
A	105	0.008	Plated	Via
B	16	0.015	Plated	Via
C	273	0.020	Plated	Via
D	2	0.063	Non-Plated	Pad
E	12	0.100	Plated	Pad
F	2	0.125	Plated	Pad

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UNLESS OTHERWISE  
SPECIFIED: DIMENSIONS  
ARE IN INCHES

TOLERANCES  
.XX = ±.01  
.XXX = ±.005  
.XXXX = ±.0010  
ANGLES = ± 0.5°

INTERPRET DRAWING  
PER ANSI/ASME Y14.5 - 2009



THIRD ANGLE PROJECTION  
DO NOT SCALE DRAWING


SAP NO. 289638

APPROVAL AND RELEASE  
RECORDS MAINTAINED IN PDE

DESIGNER T. THOMAS  
ENGR. S. SCHAFER

PDE CONTROLLED

CAGE CODE  
1CVM1

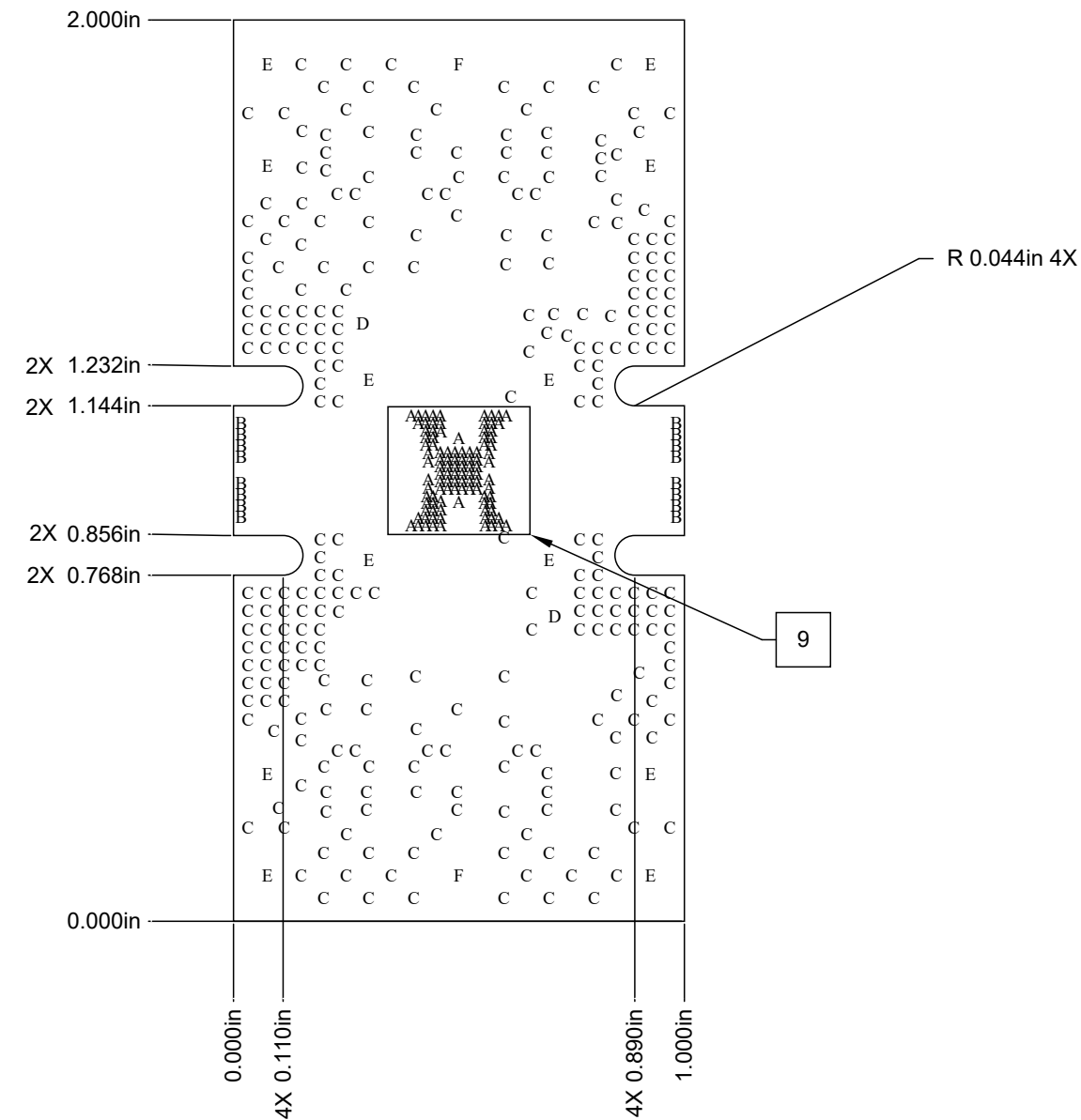


TITLE:  
QPA1022 EVAL PCB  
DESIGN PACKAGE

SIZE B  
DWG. NO. QPA1022-4000  
REV. B

SCALE: 1:1  
SHEET 1 OF 3

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
B	SOLDER MASK CHANGE FOR C1,C2,C5, AND C6	04/30/19	T.THOMAS



4

3

2

1

D

D

C

C

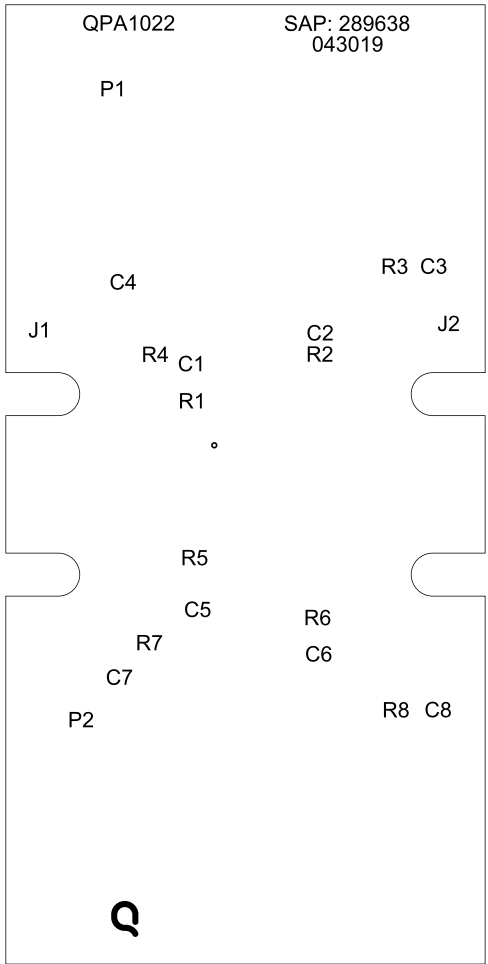
B

B

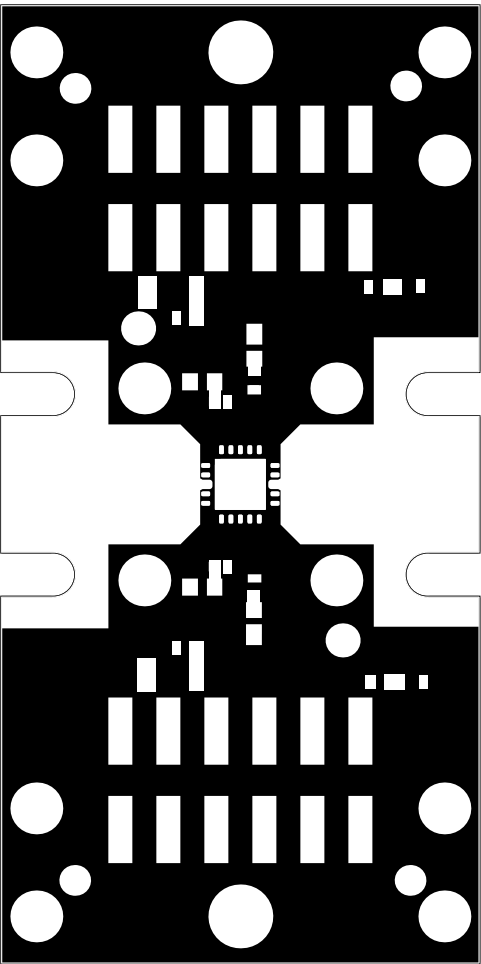
A

A

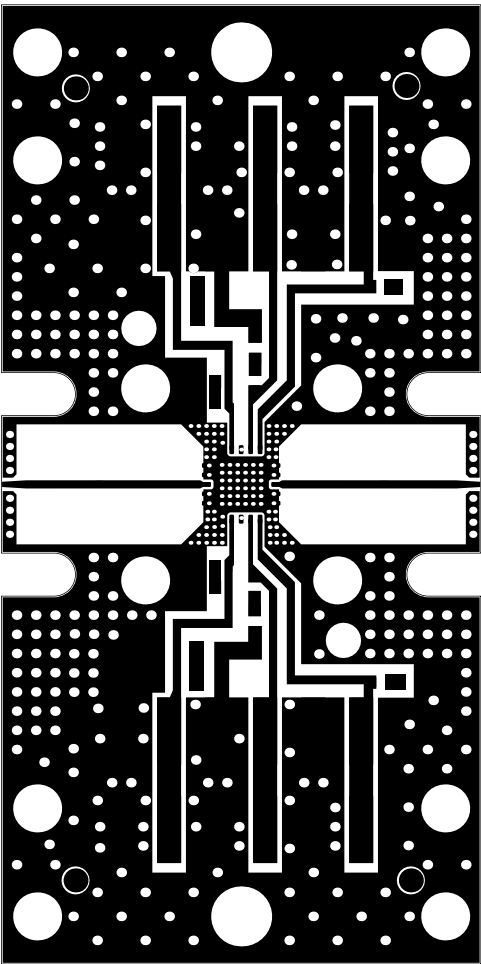
SILKSCREEN TOP



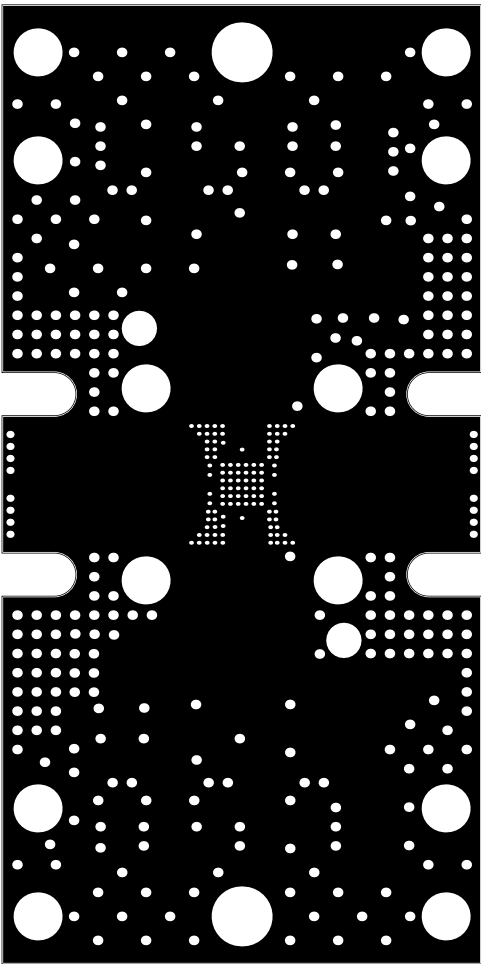
SOLDERMASK TOP



METAL 1 TOP



METAL 2 BOTTOM



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SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	QPA1022-4000	B
SCALE:	1:1	SHEET 2 OF 3	

4

3

2

1

D

D

C

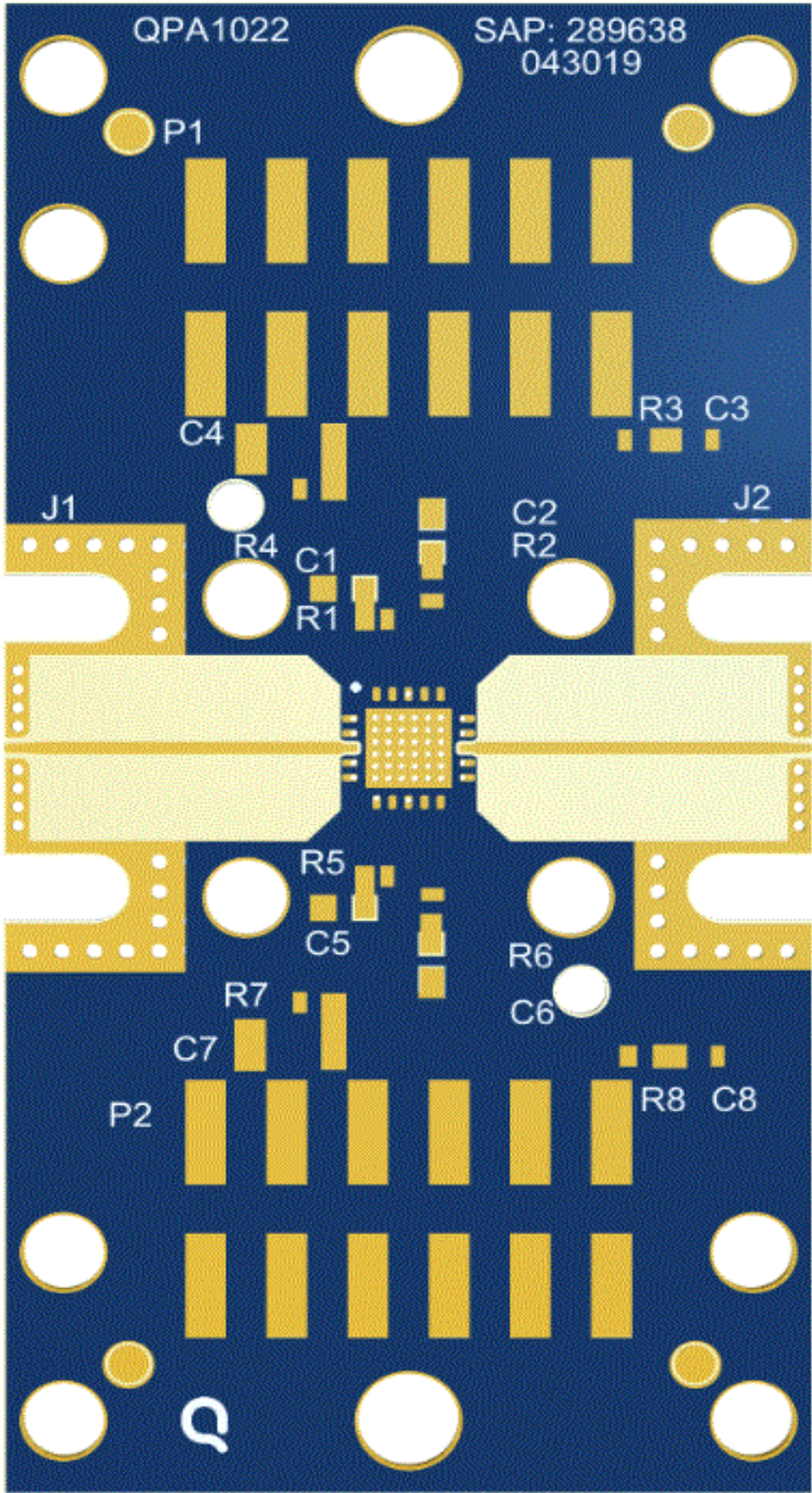
C

B

B

A

A



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SIZE	CAGE CODE	DWG. NO.	REV.
B	1CVM1	QPA1022-4000	B
SCALE: 1:1		SHEET 3 OF 3	